COMPARATIVE ANALYSIS OF VARIOUS ALGORITHM OF ADDLL

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ABSTRACT
Delay lines are devices that introduce time delay to signals by a pre-determined time constant. They are characterized by their delay step, jitter performance and delay range. The delay step is a measure of the finest incremental time step a delay line can produce, while the delay range is the maximum time a signal can be delayed.
A delay locked loop is a feedback control system that equalizes the phase of two delayed copies of the same clock signal. As compared to DLL,ADDLLs require few thousands gates and the area is scaled at each technology generation. By this paper, comparative analysis of various algorithms used for ADDLL has been done.
Keywords: DLL, ADDLL, VSAR

INTRODUCTION

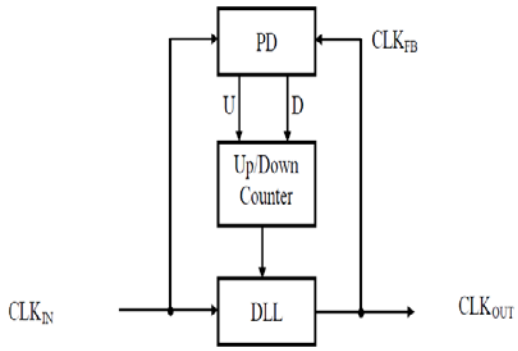
A DLL can be used to synchronize the phase of the clock that is distributed by the clock to the clock inputs of all flip-flips within the core of the IC. The common approach for clock processing, such as de-skewing and frequency multiplication, is based on Delay Locked Loops (DLLs). A DLL plays an important role in digital system design.
In All Digital Delay Locked Loops (ADDLLs), voltage level can be scaled to very low levels, by using CMOS gates. They are also portable to structured arrays and gate arrays merely by routing the existing gates in the arrays.

ALGORITHM FOR ADDLL

There are mainly two controlling algorithms for All-Digital Delay Locked Loop (ADDLL):

Basic counter type algorithm

In this algorithm, there is implementation of counter type control algorithm with feedback so that a desired phase relationship between an input clock (CLK_{IN}) and a feedback clock (CLK_{FB}) can be made. The main working takes place via two error signals (D and U), which defines the relation of the feedback clock (CLK_{FB}) with the input clock (CLK_{IN}).

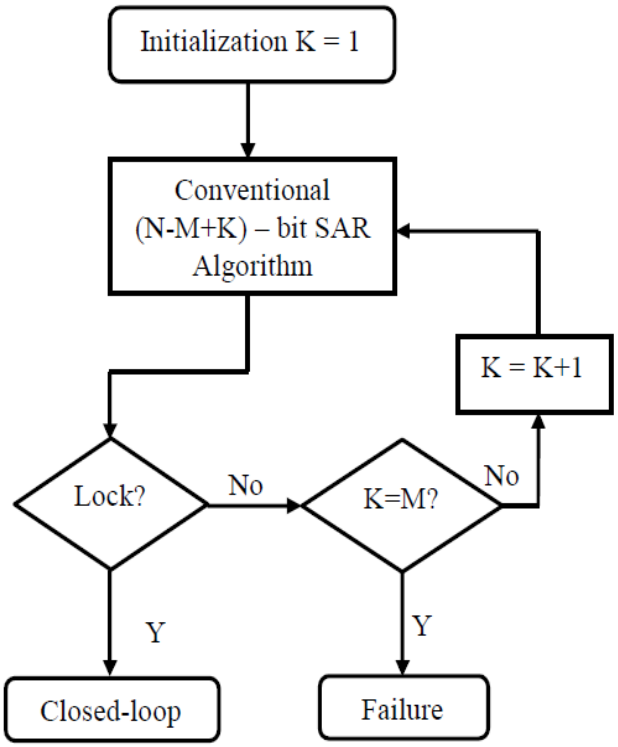


Basic counter type algorithm

The value of counter increments (decrements) to increase (decrease) the delay through the programmable delay line, whenever there is any change in U or D signal.

Variable SAR algorithm

Variable successive approximation register controlled algorithm aims in performing binary search without the harmonic-locking issue. The delay produced by the delay line should be such that CLKFB should not exceed the comparison point.
For the VSAR controller, the delay of the delay line increases gradually from the minimum and never exceeds twice the input clock period. The flowchart of VSAR algorithm is shown.It consist of an M-bit VSAR unit and an (N-M)-bit conventional SAR unit, where N is the total number of control bits for the digital-controlled delay line (DCDL).



VSAR algorithm

The comparison of values of various parameters obtained using different algorithms for ADDLL is shown with the help of following table-

Parameter	VSAR	Counter
Digital Technology	TSMC 0.18um	TSMC 0.18um
Lock range (operating frequency range) in MHz	14 to 170	14 to 170
Total No. of cells Cell Area(Sq.um)	1760 8967	1585 15448
Leakage Power(nW) Internal Power(nW) Net Power(nW) Switching Power(nW)	163.819 12996150.015 13649589.053 26645739.068	91.690 12278730.920 13324282.102 25603013.022
Max. jitter	<251.8ps	<251.8ps

CONCLUSION

As compared to Basic Counter algorithm, VSAR algorithm is more efficient in terms of power ratings and delay.

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